UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,164	02/15/2002	Yasumitsu Miyahara	NEC IPS-2157	1281

27667 7590 06/13/2005

HAYES, SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701

EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,164	MIYAHARA, YASUMITSU	
	Examiner	Art Unit	
	Ejaz Naheed	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 43791/2001, filed on 02/20/2001.

Specification

2. The abstract of the disclosure is objected to because it misspelled 'shift' to 'shit' (see line 12). Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Banavong et al. (5,640,424), hereafter referred to as Banavong.

Refer to claim 1, Banavong discloses, 'a digital signal processing apparatus comprising: an A/D converter for converting an analog input signal into a digital signal' (see figure 5, element 66, col.6, lines 27-29), 'a digital filter for performing half-band processing to a sampling output of a digital signal outputted by said A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output' (see figure 5, elements 76 and

78, col.7, lines 4-10;48-50), 'and an anti-aliasing circuit' (see figure 5, elements 84 and 86), 'for suppressing or removing noise having an aliasing band, which is caused by the half-band processing in said digital filter, by using a sign signal outputted from said digital filter' (see figure 5, col.7, lines 21-53).

Refer to claim 2, Banavong teaches, 'wherein said anti-aliasing circuit determines whether the output from said digital filter, which is subjected to said half-band processing, is a pass signal having the normal band or a pass signal having the aliasing signal, based on a changing period of the sign signal outputted from said digital filter, and suppresses or removes only the pass signal having the aliasing band' (see figure 5, element 54, col.7, lines 19-35).

Refer to claim 3, Banavong discloses, 'the apparatus according to claim 1, wherein said anti-aliasing circuit comprises: a period measuring circuit for measuring a changing period of the sign signal outputted by said digital filter' (see figure 9a, col.6, lines 24-26), 'a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band' (see figure 9b, col.6, lines 17-26), 'a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold which is set to said threshold holding circuit and for outputting a shift control signal when it is determined that the period measured by said period measuring circuit is not larger than the threshold' (see figure 9a, col.6, lines 17-26), 'and a shift register for shifting a signal which is inputted from said digital filter and is stored, based on said shift control signal,

and for suppressing an amplitude of the aliasing noise' (see figure 7 and 9b, col.7, lines 40-48).

Refer to claim 4, Banavong inherently teaches, 'a shift value setting register, to which the number of shift bits is set when the signal, which is inputted from said digital filter and is stored, is subjected to shift processing by said shift register'.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 and 6 are rejected under 35 U.S.C 103(a) as being unpatentable over Banavong et al. (5,640,424), hereafter referred to as Banavong, in view of Ikeda (US 6,285,768).

Refer to claim 5, Banavong teaches all the limitations of the claim invention but he fails to disclose a delay circuit.

However, Ikeda discloses 'a delay circuit (see figure 2, elements 3,8,9,11 and 17) for delaying the output from said digital filter by a delay time (see figure 2, elements 3, 8, 9, 11 and 12, col.4, lines 1-22) which is taken by the measurement by said period measuring circuit (see figure 2, elements 14 and 15, col.5, lines 14-19) and the comparison calculation by said comparator' (see figure 2, element 18).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ikeda into Banavong as to perform signal to noise ratio estimation correctly

and speedily and generate a smaller after convergence distortion as taught by Ikeda (see col.6, lines 55-59).

Refer to claim 6, Banavong discloses, 'a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter (see figure 9a, col.6, lines 24-26), 'a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band (see figure 9a or 9b, col.6, lines 17-26), 'a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set to said threshold holding circuit and for outputting a clear signal when it is determined that the period is not larger than the threshold' (see figure 9a, col.6, lines 17-26).

However, Banavong fails to disclose a delay circuit.

Ikeda discloses, 'a delay circuit for delaying the output from said digital filter by a delay time (see figure 2, elements 3, 8, 9, 11, 12, and 17, col.4, lines 1-22) which is taken by the measurement of said period measuring circuit (see figure 2, elements 14 and 15 combined, col.5, lines 14-19) and the comparison calculation of said comparator and for erasing a signal during delay processing when said clear signal is inputted' (see figure 2, element 18, col.5, lines 53-60).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ikeda into Banavong as to perform signal to noise ratio estimation correctly and speedily and generate a smaller after convergence distortion as taught by Ikeda (see col.6, lines 55-59).

7. Claims 7 is rejected under 35 U.S.C 103(a) as being unpatentable over Banavong et al. (5,640,424), hereafter referred to as Banavong, in view of Horiike et al. (5,548,619), hereafter referred to as Horiike, and further in view of De Jaeger (4,433,425).

As per claim 7, Banavong discloses, 'A digital signal processing apparatus comprising: an A/D converter for converting an analog input signal into a digital signal' (see figure 5, element 66, col.6, lines 27-29), 'a digital filter for performing half-band processing to a sampling output of a digital signal outputted by said A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output' (see figure 5, elements 76 and 78, col.6, lines 37-38).

However, Banavong fails to disclose an edge-detection circuit connected to digital filter and a period measuring circuit.

Horiike discloses, 'an edge-detection circuit (see figure 2 and 11, element 17, col.12, lines 23-33) for detecting an edge of a sign signal which is outputted by said digital filter and for generating a set pulse (see figure 2, element 14, col. 8, lines 34-63); a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter (see figure 2 and 11, element 18, col. 11, lines 18-30).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Horiike into Banavong as to perform the level detection at a signal interval modulation with a bit synchronization signal as taught by Horiike (see col.12- lines 34-45).

However, Banavong and Horiike fail to disclose a circuitry which includes threshold connected to comparator and detection register explicitly.

De Jaeger discloses, 'a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band' (see figure 3, element 406, col.11, lines 26-31) 'a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold held by said threshold holding circuit and for outputting a reset pulse when it is determined that the period is not larger than the threshold (see figure 3, element 406, col. 11, lines 26-31), 'and a detection register (see figure 3, element 403 or 407) for inputting said set pulse so as to be in a set state and outputting a first level and for inputting said reset pulse so as to be in said reset state and outputting a second level' (see figure 3, col.11, lines 31-60).

It would have been obvious to one of ordinary skill in the art to implement the teaching of De Jaeger into Horiike and Banavong as to reduce the width of the filter as taught by De Jaeger (see col. 11 lines 1-17 and lines 45-46).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Tsuda reference, 5,974,098, published on 10/26/1999 "Received Signal Detector For Digital Demoduator" and The Depinto reference, 6,041,250, published on 03/21/2000, "Adaptive Line Noise Canceler and Detector for ECG Signals".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naheed Ejaz
Examiner
Art Unit 2631

5/31/2005

EMMANUEL BAYARD
PRIMARY EXAMINER